FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  \( V_{OUT}/V_{IN} = R_F \), Current Input
  \( V_{OUT}/V_{IN} = R_F/R_{IN} \), Voltage Input
- 100% TESTED FOR BREAKDOWN:
  750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE: 0.3\( \mu \)A, max, at 240V/60Hz
- WIDE BANDWIDTH: 60kHz
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer Sensing
  (Thermocouples, RTD, Pressure Bridges)
  4mA to 20mA Loops
  Motor and SCR Control
  Ground Loop Elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The ISO100 is an optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3\( \mu \)A at 250V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since \( V_{OUT} \) of the ISO100 is simply \( I_{REF}R_F \), gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.
## SPECIFICATIONS

### ELECTRICAL

At \( T_A = +25^\circ C \) and \( \pm V_{CC} = 15\text{DC} \), unless otherwise specified.

### ISOLATION

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
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<td>750</td>
<td></td>
<td></td>
<td>2500</td>
<td></td>
<td></td>
<td>V</td>
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<td></td>
<td>2500</td>
<td></td>
<td></td>
<td>V</td>
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<td>pA/V</td>
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<td>dB</td>
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<tr>
<td>AC</td>
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<td>400</td>
<td></td>
<td></td>
<td>108</td>
<td></td>
<td></td>
<td>pA/V</td>
</tr>
<tr>
<td>Impedance</td>
<td></td>
<td>10(2)</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Leakage Current</td>
<td></td>
<td>240Vrms, 60Hz</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA, rms</td>
</tr>
</tbody>
</table>

### OFFSET VOLTAGE (RTI)

| INPUT STAGE (V_{OI})       |            | 500 | 300 | 200 | 5   |     |     | µV    |
| vs Temperature             |            | 2   |     |     | 2   |     |     | µV/kHz |
| vs Input Power Supplies    |            | 105 |     |     |     |     |     | µV/V  |
| vs Time                    |            | 1   |     |     |     |     |     | µV/kHz |
| OUTPUT STAGE (V_{OS})      |            | 500 | 300 | 200 | 5   |     |     | µV    |
| vs Temperature             |            | 2   |     |     | 2   |     |     | µV/kHz |
| vs Output Power Supplies   |            | 105 |     |     |     |     |     | µV/V  |
| vs Time                    |            | 1   |     |     |     |     |     | µV/kHz |
| Common-Mode Rejection Ratio (2) | 30Hz, R_F = 1MΩ | 3   |     |     |     |     |     | nA/V  |
| Common-Mode Range          |            | ±10 |     |     |     |     |     | V     |

### REFERENCE CURRENT SOURCES

| Magnitude                  |            | 10.5 | 12 | 12.5 | 300 | 200 | µA |
| vs Temperature             |            | 300 |     |     |     |     | ppm/°C |
| vs Power Supplies          |            | 0.3 |     |     |     |     | nA/V |
| Matching                   |            | 50  |     |     |     |     | nA  |
| vs Temperature             |            | 150 |     |     |     |     | ppm/°C |
| vs Power Supplies          |            | 0.3 |     |     |     |     | nA/V |
| Compliance Voltage         |            | −10 | +15 |     |     |     | V  |
| Output Resistance          |            | 2 x 10^4 |     |     |     |     | Ω  |

### FREQUENCY RESPONSE

| SMALL SIGNAL BANDWIDTH     | Gain = 1V/µA | 60 |     |     |     | kHz |
| FULL POWER BANDWIDTH       | Gain = 1V/µA, V_O = ±10V | 5 |     |     |     | kHz |
| Slew Rate                  |              | 0.22 | 0.31 |     |     | V/µs |
| SETTLING TIME              |              | 0.1% | 100 |     |     | µs  |

### TEMPERATURE RANGE

| Specification              | −25 | +85 |     |     |     |     | °C |
| Operating                 | −40 | +100 |     |     |     |     | °C |
| Storage                   | −40 | +100 |     |     |     |     | °C |

### UNIPOLAR OPERATION

| GAIN                       |              | 2 | 5 | 1 | 2 | 1 | 2 | % of FS |
| INITIAL ERROR (adjustable to zero) | V_O = R_F (I_{IN}) | 0.03 | 0.07 | 0.01 | 0.05 | 0.005 | 0.03 | %/°C |
| vs Temperature             |              | 0.05 |     |     |     |     | %/kHz |
| vs Time                    |              | 0.1 |     |     |     |     | %/kHz |
| Nonlinearity (2)           |              | 0.1 | 0.4 | 0.03 | 0.1 | 0.02 | 0.07 | %   |

### CURRENT NOISE

| 0.01Hz to 10Hz              | 20 |     |     |     |     |     | pA-p |
| 10Hz                       | 1  |     |     |     |     |     | pA/V  |
| 100Hz                      | 0.7 |     |     |     |     |     | pA/V  |
| 1kHz                       | 0.65 |     |     |     |     |     | pA/V  |
## ELECTRICAL

At $T_a = +25\, ^\circ C$ and $\pm V_{CC} = 15\, \text{VDC}$, unless otherwise specified.

### INPUT OFFSET CURRENT ($I_{OS}$)

<table>
<thead>
<tr>
<th>PARAMETER CONDITIONS</th>
<th>ISO100AP</th>
<th>ISO100BP</th>
<th>ISO100CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Offset</td>
<td>1</td>
<td>10</td>
<td>*</td>
</tr>
<tr>
<td>vs Temperature</td>
<td>0.05</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>vs Power Supplies</td>
<td>0.1</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>vs Time</td>
<td>100</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

### POWER SUPPLIES

#### Input Stage
- Voltage (rated performance): $\pm 15\, \text{V}$
- Supply Current: $I_N = -0.02\, \mu\text{A}$
- Voltage (derated performance): $+8, -1.1\, \mu\text{A}$

#### Output Stage
- Voltage (rated performance): $\pm 15\, \text{V}$
- Supply Current: $V_O = 0\, \Omega$
- Short Circuit Current Limit: $\leq 40\, \text{mA}$

### GENERAL PARAMETERS

#### Input Current Range
- Linear Operation: $-10, +10\, \mu\text{A}$
- Without Damage: $-1, +1\, \mu\text{A}$

#### Input Impedance
- $R_L = 2k\, \Omega, R_F = 1M\, \Omega$
- $-10, +10\, \mu\text{A}$

#### Output Voltage Swing
- $+2, -1.1\, \mu\text{A}$

#### Output Impedance
- $1200\, \Omega$

### GAIN

#### Initial Error (Adjustable To Zero)
- $V_O = R_F \times I_{IN}$
- $2, 5, 1, 2, 1, 2, 0.03, 0.07, 0.01, 0.05, 0.005, 0.03\%$ of FS

#### vs Temperature
- $0.03, 0.07, 0.01, 0.05, 0.005, 0.03\%/\, ^\circ C$

#### vs Bias
- $0.5, 0.4, 0.03, 0.1, 0.02, 0.07\%$

### CURRENT NOISE

#### $I_{IN} = 0.2\, \mu\text{A}$
- $0.01\, \text{Hz}$ to $10\, \text{Hz}$: $1.5, *$ of FS
- $10\, \text{Hz}$: $17, *$ of FS
- $100\, \text{Hz}$: $7, *$ of FS
- $1\, \text{kHz}$: $6, *$ of FS

### INPUT OFFSET CURRENT ($I_{OS}$, bipolar$^4$)

#### Initial Offset
- $40, 200, 20, 70, 10, 35\, \text{nA}$

#### vs Temperature
- $3, 2, 1\, \text{nA}/^\circ \text{C}$

#### vs Power Supplies
- $0.7, *$ of FS

#### vs Time
- $250, *$ of FS

### POWER SUPPLIES

#### Input Stage
- Voltage (rated performance): $\pm 15\, \text{V}$
- Supply Current: $I_N = +10\, \mu\text{A}$

#### Output Stage
- Voltage (rated performance): $\pm 15\, \text{V}$
- Supply Current: $V_O = 0\, \Omega$

### NOTES:
1. See Typical Performance Curves for temperature effects.
2. See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors.
3. Nonlinearity is the peak deviation from a “best fit” straight line expressed as a percent of full scale output.

* Same as ISO100AP.

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**PIN CONFIGURATION**

Bottom View

1. **ISO100**
2. Input Common
3. **+VCCA2**
4. **VOUT**
5. **-VCCA2**
6. **Ref1**
7. **+In**
8. **Bal**
9. **-VCCA1**
10. **NC**(1)
11. **Bal**
12. **Ref2**
13. **NC**(1)
14. **Bal**
15. **+In**
16. **Ref1**
17. **-In**
18. **Input Common**

**NOTE:** (1) No internal connection.

---

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltages ................................................................. ±18V
Isolation Voltage, AC pk or DC .................................................... 750V
Input Current ................................................................................ ±1mA
Storage Temperature Range ........................................... –40°C to +100°C
Lead Temperature (soldering, 10s) ............................................. +300°C
Output Short-Circuit Duration ........................................... Continuous to Ground

---

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO100AP</td>
<td>18-Pin Bottom-Braze DIP</td>
<td>–25°C to +85°C</td>
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<tr>
<td>ISO100BP</td>
<td>18-Pin Bottom-Braze DIP</td>
<td>–25°C to +85°C</td>
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<td>ISO100CP</td>
<td>18-Pin Bottom-Braze DIP</td>
<td>–25°C to +85°C</td>
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**ABSOLUTE MAXIMUM RATINGS**

**PACKAGE INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>PACKAGE DRAWING NUMBER(1)</th>
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<tbody>
<tr>
<td>ISO100AP</td>
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<tr>
<td>ISO100BP</td>
<td>18-Pin Bottom-Braze DIP</td>
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</tr>
<tr>
<td>ISO100CP</td>
<td>18-Pin Bottom-Braze DIP</td>
<td>220</td>
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</tbody>
</table>

**NOTE:** (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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**ELECTROSTATIC DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ C$, $\pm V_{CC} = 15VDC$, unless otherwise specified.

**SMALL SIGNAL FREQUENCY RESPONSE**

**BIPOLAR OUTPUT SWING vs $R_F$**

**BIPOLAR INPUT STAGE SUPPLY CURRENT vs INPUT CURRENT**

**UNIPOLAR OUTPUT SWING vs $R_F$**

**PHASE SHIFT vs FREQUENCY**

**UNIPOLAR INPUT STAGE SUPPLY CURRENT vs INPUT CURRENT**
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $\geq V_{CC} = 15\text{VDC}$, unless otherwise specified.

**ISOLATION LEAKAGE CURRENT vs ISOLATION VOLTAGE**

- AC Leakage Current (µA RMS)
- DC Leakage Current (pA)
- Isolation Voltage (kV)

**CONTINUOUS DC ISOLATION VOLTAGE vs TEMPERATURE**

- Continuous DC Isolation Voltage (V)
- Temperature ($^\circ\text{C}$)

**AC ISOLATION VOLTAGE vs TEMPERATURE**

- AC Isolation Voltage (Vp)
- Temperature ($^\circ\text{C}$)

**RATE OF GAIN ERROR SHIFT vs ISOLATION VOLTAGE**

- Rate of Change of Gain Error (%/hr)
- Temperature ($^\circ\text{C}$)

**GAIN ERROR vs TEMPERATURE AND ISOLATION VOLTAGE**

- Gain Error (Normalized to $+25^\circ\text{C}$)
- Temperature ($^\circ\text{C}$)

**NOTES:**
- $V_M$ and $T_T$ approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.
- $T_T = +65^\circ\text{C}$, $V_T = 200\text{VDC}$. Shift does not occur for AC voltages.

- $V_M < V_T$
- $V_M > V_T$
THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications, an output voltage is obtained by passing the output current through the feedback resistor \( R_F \).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors coupled together to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. \( I_{\text{REF1}} \) and \( I_{\text{REF2}} \) are required only for bipolar operation to generate a midscale reference. The LED and photodiodes \( (D_1 \text{ and } D_2) \) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around \( A_1 \) occurs through the optical path formed by the LED and \( D_1 \). The signal is transferred across the isolation barrier by the matched light path to \( D_2 \).

The overall isolation amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, \( I_{\text{IN}} \), flows out of the ISO100 (\( I_{\text{IN}} \) must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of \( A_1 \) increases, driving current through the LED. As the LED light output increases, \( D_1 \) responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (–Input to \( A_1 \)) is zero. At that point, the negative feedback through \( D_1 \) has stabilized the loop, and the current \( I_{\text{IN}} \) equals the input current plus the bias current. As a result, no bias current flows in the source. Since \( D_1 \) and \( D_2 \) are matched \( (I_{D1} = I_{D2}) \), \( I_{\text{IN}} \) is replicated at the output via \( D_2 \). Thus, \( A_1 \) functions as a unity-gain current amplifier, and \( A_2 \) is a current-to-voltage converter, as described below.

Current produced by \( D_2 \) must either flow into \( A_2 \) or \( R_F \). Since \( A_2 \) is designed for low bias current \( (\approx 10nA) \), almost all of the current flows through \( R_F \) to the output. The output voltage then becomes:

\[
V_O = (I_{D2})R_F = (I_{D1} \pm I_{OS})R_F = -(I_{\text{IN}})R_F = I_{\text{IN}}R_F \tag{1}
\]

where, \( I_{OS} \) is the difference between \( A_1 \) and \( A_2 \) bias currents. For input voltage operation \( I_{\text{IN}} \) can be replaced by a voltage source \( (V_{IN}) \) and series resistor \( (R_{IN}) \), since the summing node of the op amp is essentially at ground. Thus, \( I_{\text{IN}} = V_{IN}/R_{IN} \).

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from \( A_1 \) to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met, the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1 are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation.

FIGURE 1. Simplified Block Diagram of the ISO100.
The output then becomes:

$$V_{OUT} = R_F \left( \frac{V_{IN} \pm V_{OS}}{R_{IN}} - I_{REF1} \pm I_{OS}(1 + A_e) + I_{REF2} \right) \pm V_{OSO}$$\\
\hspace{1cm} (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} = R_F \left( \frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS \, UNIPOLAR} \right) \pm V_{OSO}$$\\
\hspace{1cm} (3)$$

This voltage is then referred back to the input by dividing by $R_F/R_{IN}$.

$$V_{OS \, (RTI)} = (\pm V_{OSI}) \pm R_{IN} (I_{OS \, UNIPOLAR}) + V_{OSO}(R_F/R_{IN})$$\\
\hspace{1cm} (4)$$

**Example 1.** Refer to Figure 2 and Electrical Specifications Table.

Given:

- $I_{OS \, BIPOLAR} = +35nA$
- $R_{IN} = 100k\Omega$
- $R_F = 1M\Omega$ (gain = 10)
- $V_{OSI} = +200\mu V$
- $V_{OSO} = +200\mu V$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$.

$$V_{OS \, total \, RTI} = [\pm (V_{OSI} \pm R_{IN} (V_{OSBIPOLAR}) - R_{IN} (I_{REF1}))] \]$$
$$\hspace{1cm} [1 + A_e] + R_{IN} I_{REF2} \pm V_{OSO}(R_F/R_{IN})$$
$$\hspace{1cm} = [(0.2mV + 3.5mV - 1.25V) \]$$
$$\hspace{1cm} [1.02] + 100k\Omega (12.5\mu A)] +$$
$$\hspace{1cm} 200\mu V(1M\Omega/100k\Omega)$$
$$\hspace{1cm} = [-21.2mV]$$

$$V_{OS \, total \, RTO} = V_{OS \, total \, RTI} \times R_F/R_{IN}$$
$$\hspace{1cm} = -212mV \times 10$$
$$\hspace{1cm} = -212mV$$

**DC ERRORS**

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

$A_1$ and $A_2$—assumed to be ideal amplifiers.

$V_{OSO}$ and $V_{OSI}$—the input offset voltages of the output and input stage, respectively. $V_{OSO}$ appears directly at the output, but $V_{OSI}$ appears at the output as

$$V_{OSI} = \frac{R_F}{R_{IN}} \cdot V_{OS}$$\\
\hspace{1cm} (1)$$

$I_{OS}$—the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of $A_1$ and $A_2$ and the matching errors in the optical components in the unipolar mode.

$I_{REF1}$ and $I_{REF2}$—reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS \, BIPOLAR}$ error.

$I_{D1}$ and $I_{D2}$—currents generated by each photodiode in response to the light from the LED.

$A_e$—gain error.

$$A_e = \left| \frac{\text{Ideal gain}}{\text{Actual gain}} \right| - 1$$

**FIGURE 2.** Circuit Model for DC Errors in the ISO100.

NOTE: (1) Use 1MΩ or greater to achieve a full scale output of 10V.
NOTE: This error is dominated by $I_{OS\text{ bipolar}}$ and the reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either $R_F$ or $R_{IN}$.

**COMMON-MODE AND HIGH VOLTAGE ERRORS**

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

**Definitions of CMR and IMR**

$I_{OS}$ is defined as the input current required to make the ISO100’s output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage ($V_{CM}$) and the change in $I_{OS}$ required to maintain the amplifier’s output to zero:

\[
\text{CMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{CM}} \text{ in nA/V} \quad (5)
\]

\[
\text{CMRR (V-mode)} = \left[ \frac{\Delta I_{OS}}{\Delta V_{CM}} \right] R_{IN} = \frac{\Delta V_{ERR_{CM}}}{\Delta V_{CM}} \text{ in V/V} \quad (6)
\]

IMRR defines the relationship between a change in the applied isolation mode voltage ($V_{IM}$) and the change in $I_{OS}$ required to maintain the amplifier’s output to zero:

\[
\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{IM}} \text{ in pA/V} \quad (7)
\]

\[
\text{IMRR (V-mode)} = \left[ \frac{\Delta I_{OS}}{\Delta V_{IM}} \right] R_{IN} = \frac{\Delta V_{ERR_{IM}}}{\Delta V_{IM}} \text{ in V/V} \quad (8)
\]

CMRR and IMRR in V/V are a function of $R_{IN}$.

$V_{IM}$ is the voltage between input common and output common.

$V_{CM}$ is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

$V_{ERR}$ is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of $V_{CM}$ and $V_{IM}$.

**CMRR and IMRR** are the common-mode and isolation-mode rejection ratios, respectively.

**Total Capacitance** ($C_1$ and $C_2$) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance ($C_2$) couples to the input of the second stage, and contributes to IMRR.

**Example 2.** Refer to Figure 3 and Electrical Specification Table.

Given: $V_{CM} = 1\text{VAC peak at 60Hz}, V_{IM} = 200\text{VDC}$, $\text{CMRR} = 3\text{nA/V, IMRR} = 5\text{pA/V}$, $R_{IN} = 100\text{k}\Omega, R_F = 1\text{M}\Omega$ (Gain = 10)

Find: The error voltage referred to the input and output when $V_{IN} = 0\text{V}$

\[
V_{ERR_{RTI}} = (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN})
= 1\text{V} (3\text{nA/V})(100\text{k}\Omega)
+ 200\text{V} (5\text{pA/V})(100\text{k}\Omega)
= 0.3\text{mV} + 0.1\text{mV}
= 0.4\text{mV}
\]

\[
V_{ERR_{RTO}} = V_{ERR_{RTI}} (R_F/R_{IN})
= 0.4\text{mV} (10)
= 4\text{mV (with DC IMRR)}
\]

NOTE: This error is dominated by the CMRR term.

For purposes of comparing CMRR and IMRR directly with **dB specifications**, the following calculations can be performed:

\[
\text{CMRR in V/V} = \text{CMRR (I-mode)}(R_{IN})
= 3\text{nA/V}(100\text{k}\Omega)
= 0.3\text{mV/V}
\]

\[
\text{CMR} = 20 \log (0.3\text{mV/V}) = -70\text{dB at 60Hz}
\]

\[
\text{IMRR in V/V} = \text{IMRR (I-mode)}(R_{IN}) = 5\text{pA/V}(100\text{k}\Omega)
= 0.5\text{µV/V}
\]

\[
\text{IMR} = 20 \log (0.5 \times 10^{-6} \text{V/V}) = -126\text{dB at DC}
\]

**Example 3.**

In Example 3, $V_{IM}$ is an AC signal at 60Hz and

\[
\text{IMR} = \frac{400\text{pA}}{V}
\]

\[
V_{ERR_{RTI}} = V_{ERR_{CM}} + V_{ERR_{IM}}
= 0.3\text{mV} + 200\text{V} (400\text{pA/V})(100\text{k}\Omega)
= 8.3\text{mV}
\]

\[
V_{ERR_{RTO}} = 83\text{mV (with AC IMRR)}
\]
Example 4.
Given: Total error RTO from Examples 1 and 3 as 378mV worst case.
Find: Percent error of +10V full scale output
\[
\% \text{ Error} = \frac{V_{\text{ERR TOTAL}}}{V_{FS}} \times 100\%
\]
\[
= \frac{378 \text{mV}}{10 \text{V}} \times 100\%
\]
\[
= 3.78\%
\]

NOISE ERRORS
Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, \(C_F\) in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

OPTIONAL ADJUSTMENTS
There are two major sources of offset error: offset voltage and offset current. \(V_{OSI}\) and \(V_{OSO}\) of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that \(V_{OSO}\) (500µV, max) appears directly at the output, but \(V_{OSI}\) appears at the output multiplied by gain \((R_F/R_{IN})\). In general, \(V_{OS}\) is small compared to the effect of \(I_{OS}\) (see Example 1). To adjust for \(I_{OS}\) use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be “slightly bipolar.” By sampling the reference current with \(R_5\) and \(R_6\), the minimum current required to keep the input stage in the linear region of operation can be established. \(R_7\) and \(R_8\) are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With \(V_{IN} = \text{“open.”}\), \(I_{OS}\) is trimmed by adjusting \(R_{10}\) to make the output zero. \(R_{14}\) is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting \(R_{14}\).
FIGURE 7. Adjusting the Bipolar Errors.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultralow leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and –In (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input.

2. Use shielded or twisted pair cable at the input for long lines.

3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components and conductor patterns, should be maximized to reduce leakage and arcing.

5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.

6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.

7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.

8. The maximum output voltage swing is determined by I_{IN} and R_F.

\[ V_{SWING} = I_{IN \, MAX} \times R_F \]

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figure 12 through 18 show applications of the ISO100.

---

**FIGURE 12.** Two-Port Isolation Photodiode Amplifier Unipolar.

**FIGURE 13.** Precision Bridge Isolation Amplifier (Unipolar).

---

NOTES: (1) For isolated supplies see Figure 12. (2) In this example, the internal precision current reference, I_{REF}, provides bridge excitation. (3) Pin 8 of the INA101 must be more negative than –2mV for linear operation of the ISO100 with R_1 = 100kΩ.
FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).
FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

\[ V_O = 1M \left( \frac{V_{IN1}}{10k} + \frac{V_{IN2}}{100k} + I_{IN1} + I_{IN2} \right) \]

\[ \pm V_{CC} \text{ to input stages of amplifiers} \]

724 Isolated Power Supply

NOTE: (1) No additional connections to output amplifiers
Note that a variety of input/gain configurations can be used.
FIGURE 18. Multiple Channel Isolation Amplifier (Bipolar) with Programmable Gain (useful in data acquisition systems).

NOTE: (1) For isolated power supplies see Figures 10 and 11.
## PACKAGING INFORMATION

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<th>Orderable Device</th>
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<th>Pins</th>
<th>Package Qty</th>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
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- **TBD**: The Pb-Free/Green conversion plan has not been defined.
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- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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